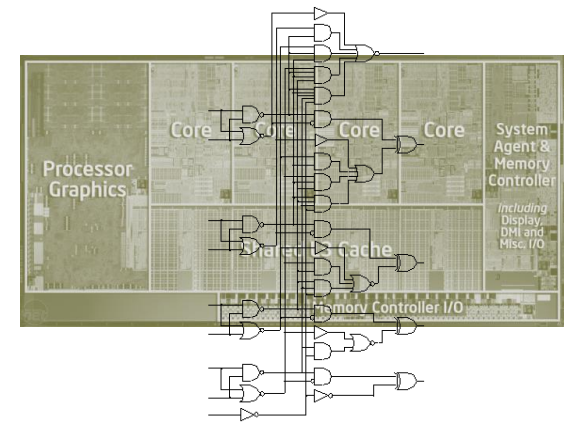




고려대학교
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COSE221, COMP211 Logic Design

Lecture 4. Sequential Logic

- Miscellaneous -

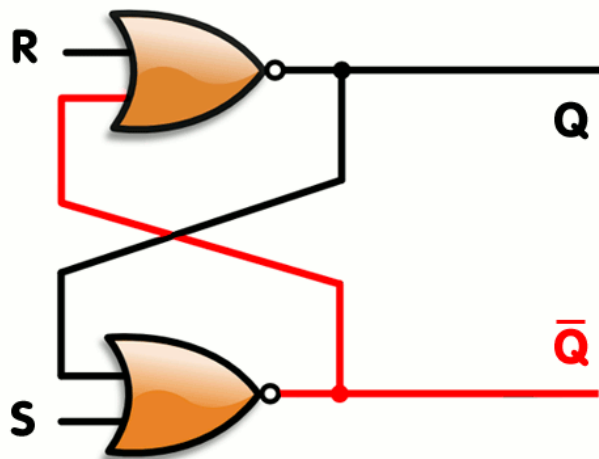
Prof. Taeweon Suh

Computer Science & Engineering

Korea University

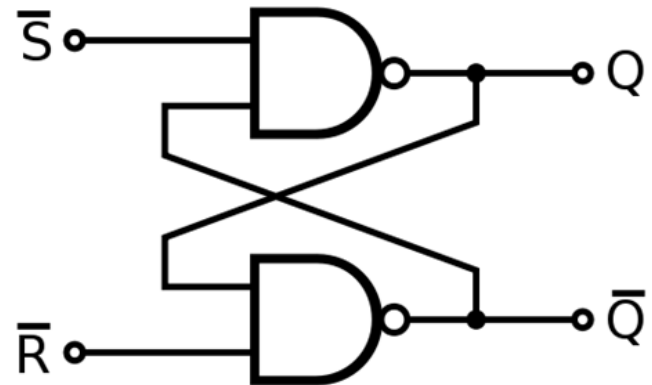
SR Latch

SR NOR Latch



S	R	Q_{next}	Action
0	0	Q	hold state
0	1	0	reset
1	0	1	set
1	1	X	not allowed

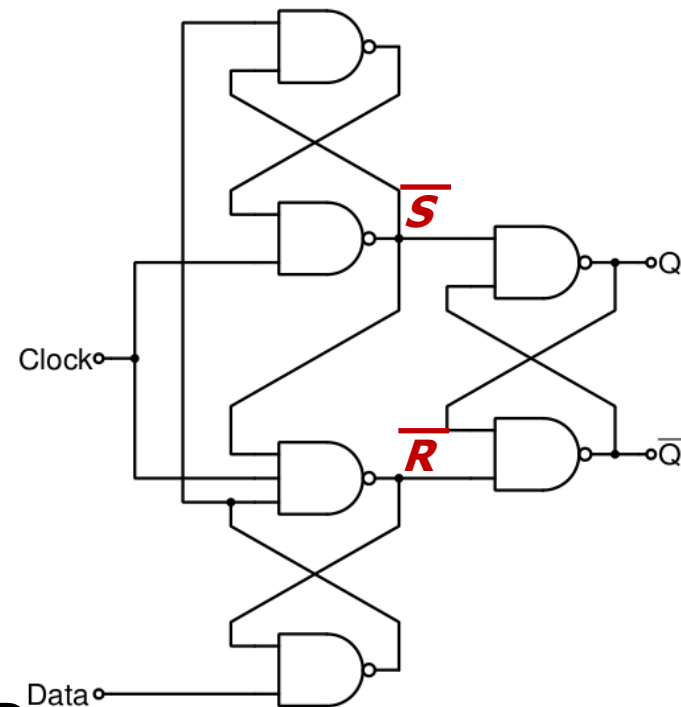
SR NAND Latch



$\bar{S}$	$\bar{R}$	Action
0	0	Restricted combination
0	1	$Q = 1$
1	0	$Q = 0$
1	1	No Change

Classical positive-edge triggered D-FF

- When clock = 0
 - $\check{S} = 1, \check{R} = 1$
- When clock goes from 0 to 1
 - If $D=0$, $\check{S} = 1$ & $\check{R} = 0$
 - If $D=1$, $\check{S} = 0$ & $\check{R} = 1$
- When clock = 1
 - The outputs keep their states regardless of data input
 - $\check{S}$ and $\check{R}$ do not change even though D changes



Async. Settable and Resettable D-FF

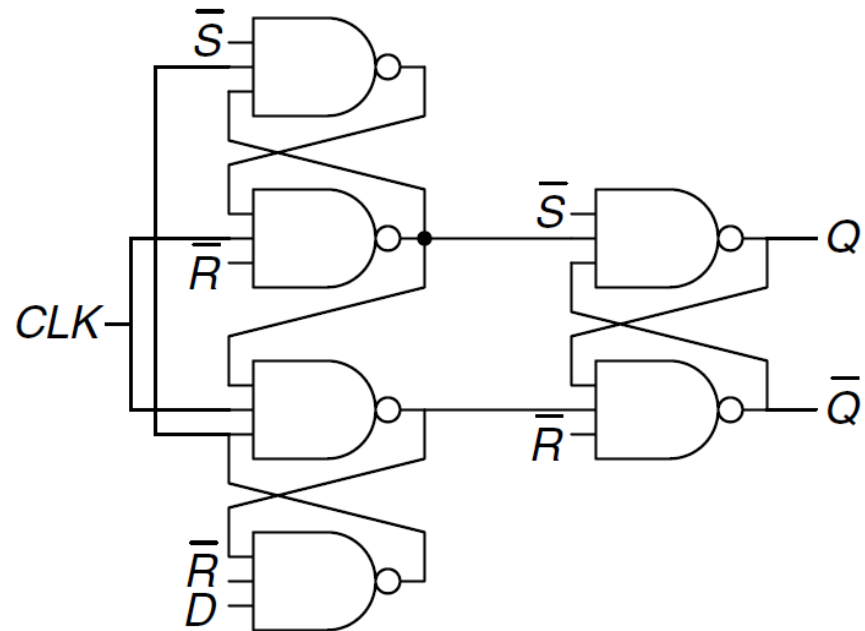
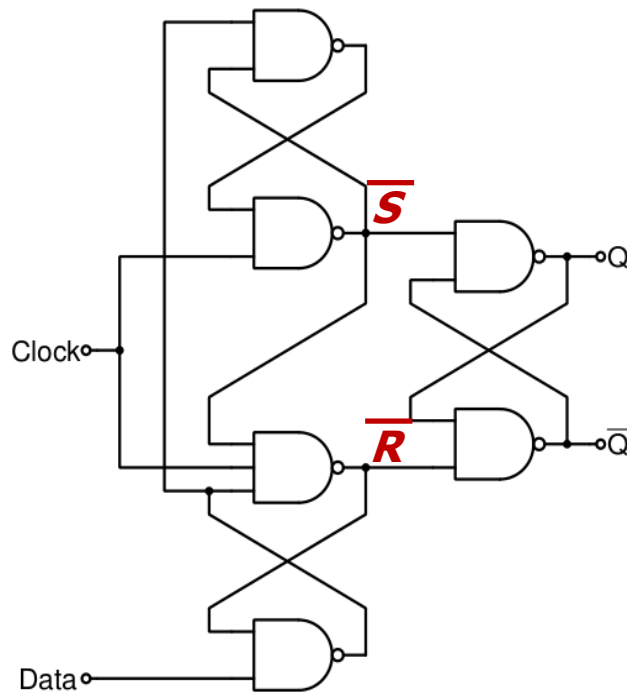
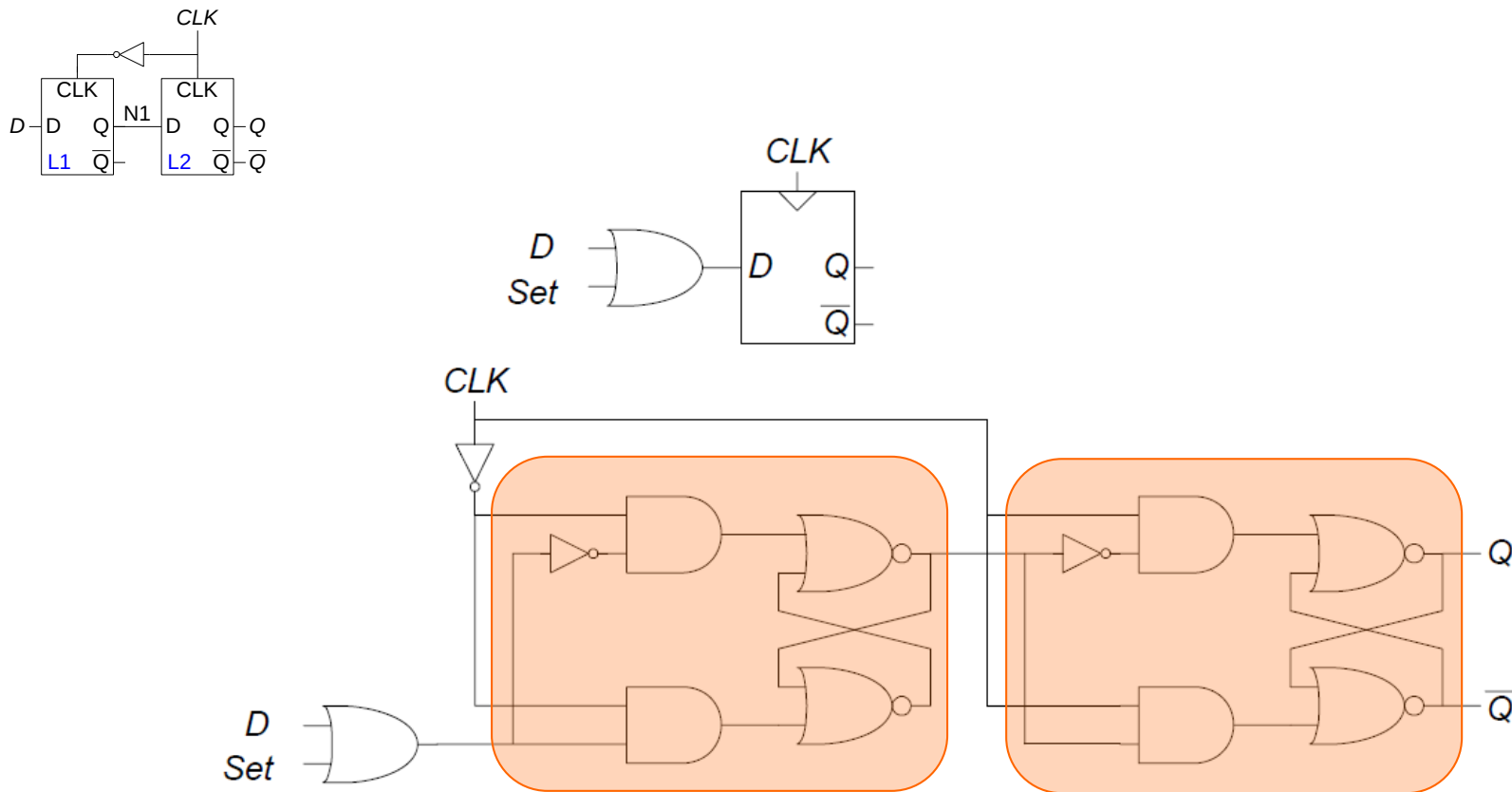
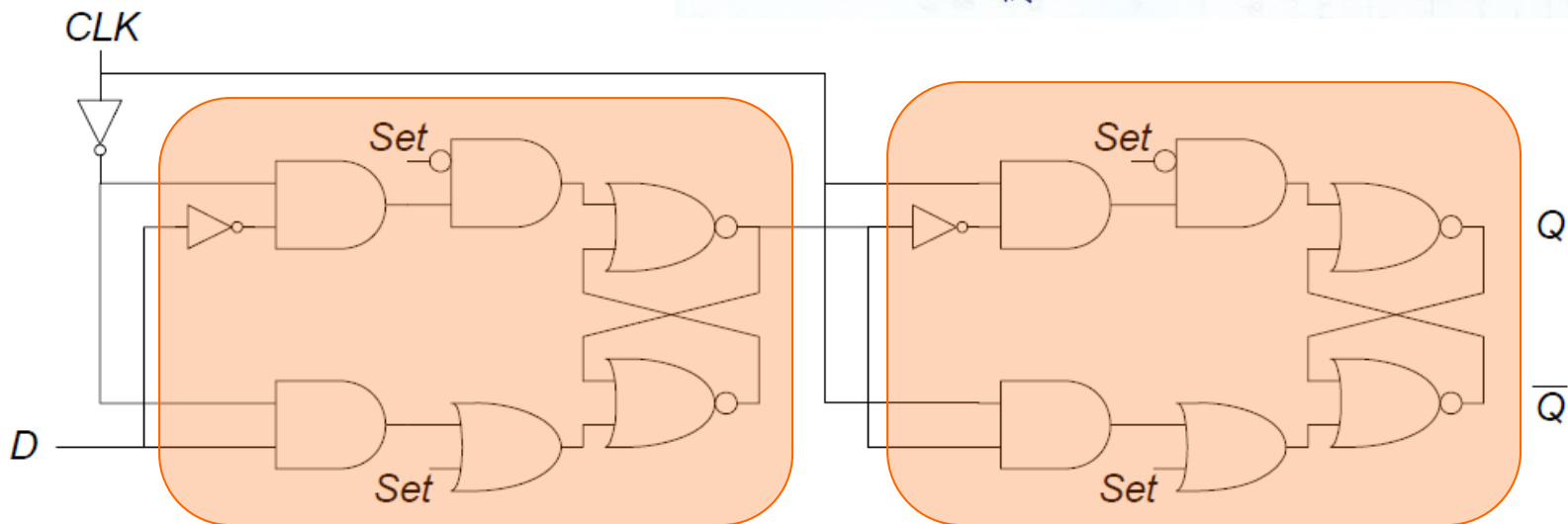
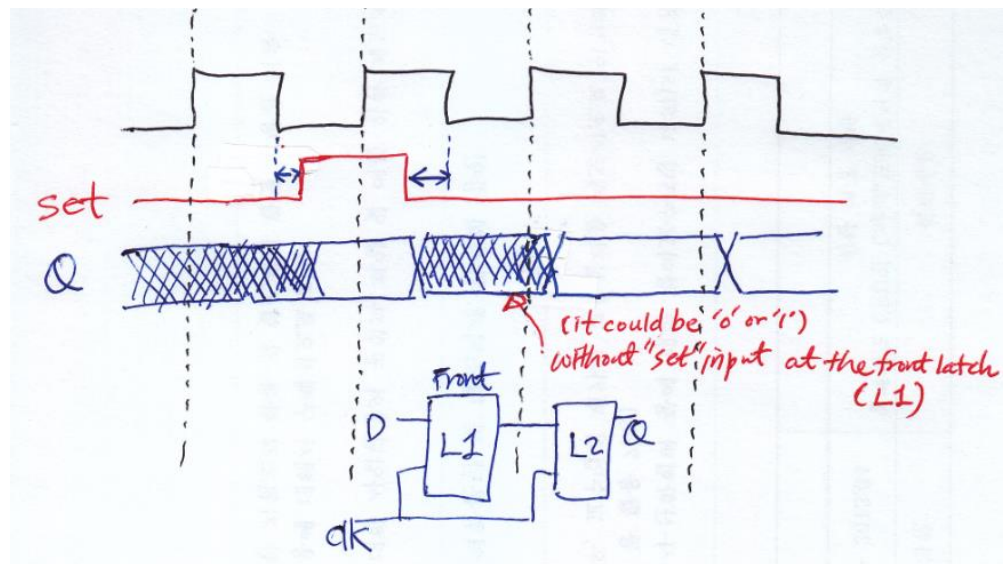
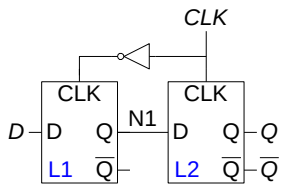


Figure 3.62 Mystery circuit

Synchronously Settable D-FF

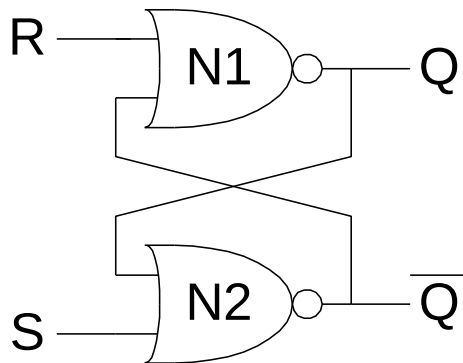


Asynchronously Settable D-FF

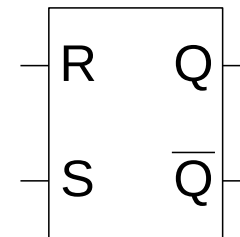


SR Latch

- One of the simplest sequential circuits is the SR (Set/Reset) latch
 - It is composed of 2 cross-coupled NOR gates
 - It has 2 inputs (S, R) and 2 outputs (Q and $\bar{Q}$)
 - When the set input (S) is 1 (and R = 0), Q is set to 1
 - **Set** makes the output (Q) to 1
 - When the reset input (R) is 1 (and S = 0), Q is reset to 0
 - **Reset** makes the output (Q) to 0

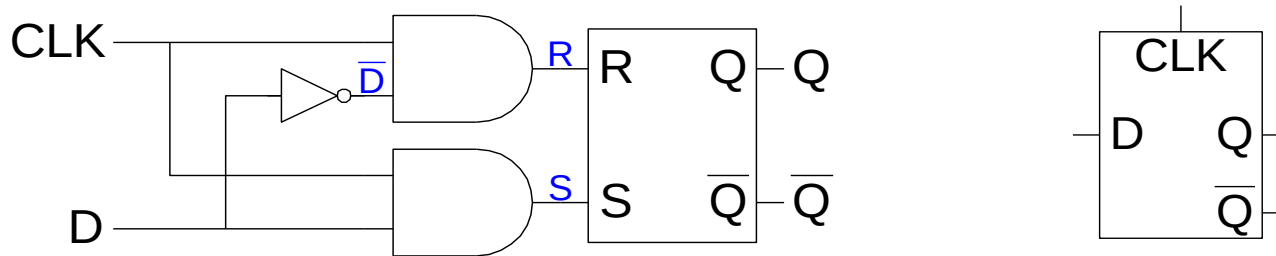


SR Latch
Symbol



D Latch Internal & Operation

- D latch operation
 - When $CLK = 1$, D passes through to Q (D latch is **transparent**)
 - When $CLK = 0$, Q holds its previous value (D latch is **opaque**)

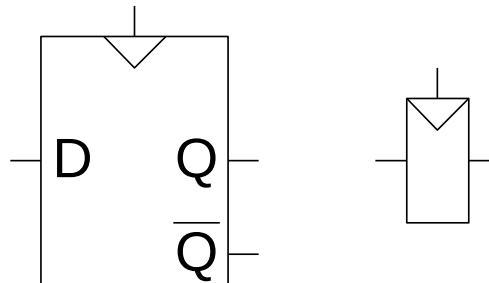


CLK	D	$\overline{D}$	S	R	Q	$\overline{Q}$
0	0	1	0	0	Q_{prev}	$\overline{Q}_{prev}$
0	1	0	0	0	Q_{prev}	$\overline{Q}_{prev}$
1	0	1	0	1	0	1
1	1	0	1	0	1	0

D Flip-Flop

- In digital logic design, it is very convenient if we can store input data at a certain moment (not during the whole time interval like D latch)
- D flip-flop provides that functionality
 - **Q changes only on the rising edge of CLK**
 - When CLK rises from 0 to 1, D passes through to Q
 - Otherwise, Q holds its previous value
- Thus, a flip-flop is called an **edge-triggered** device because it is activated on the clock edge

D Flip-Flop
Symbols



D Flip-Flop Internal Circuit

- Two back-to-back latches (L1 and L2) controlled by complementary clocks
- When $CLK = 0$
 - L1 is transparent
 - L2 is opaque
 - D passes through to N1
- When $CLK = 1$
 - L2 is transparent
 - L1 is opaque
 - N1 passes through to Q
- Thus, on the edge of the clock (when CLK rises from 0 to 1)
 - D effectively passes through to Q

